AMC597

300 MHz to 6 GHz Octal Versatile Wideband Transceiver (MIMO), UltraScale™, AMC

AMC597

Key Features

- Xilinx UltraScale™ XCKU115 FPGA
- Octo complete transceiver signal chain solution
- Four AD9371s or AD9375s on one module
- Frequency range 300 MHz to 6 GHz
- Tx synthesis bandwidth (BW) to 250 MHz
- Rx bandwidth: 8 MHz to 100 MHz
- Supports Time Division Duplex (TDD) and Frequency Division Duplex (FDD) operation
- On-board clocking or external clock with multi-transceivers synchronization capability
- Three banks of DDR4 for total 20 GB

Benefits

- High density transceiver with intensive data processing capability
- Observation channels for implementation of error correction functions
- Sniffer Receiver channels can monitor different frequency bands
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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The AMC597 is a wideband transceiver in AMC form factor. It utilizes four AD9371's connected to a Kintex UltraScale™ FPGA. This provides eight transceivers channels that make it suitable for signal SDR, BTS, antenna systems, research and instrumentation.

The onboard re-configurable UltraScale™ XCKU115 FPGA interfaces via JESD204B directly to wideband transceivers. The FPGA has interface to three banks of DDR4 memory. This allows for maximum buffer sizes to be stored during processing as well as for queuing the data to the host.

Figure 1: AMC597

Block Diagram

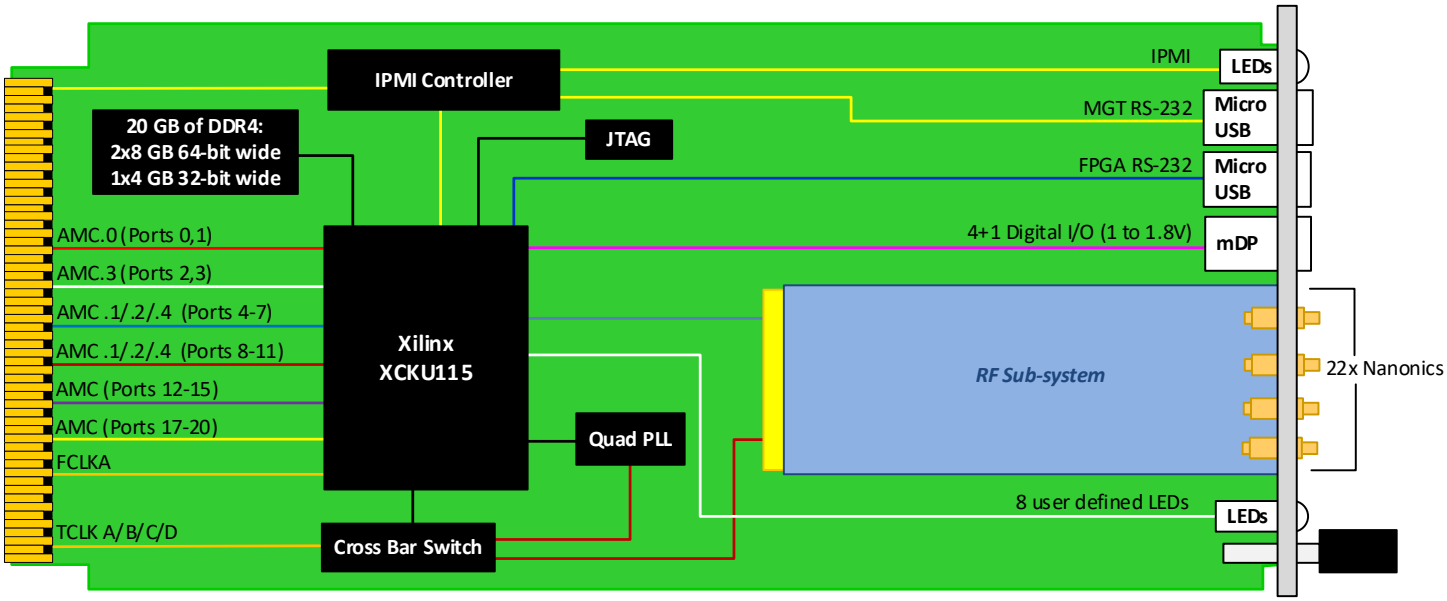


Figure 2: AMC597 Functional Block Diagram

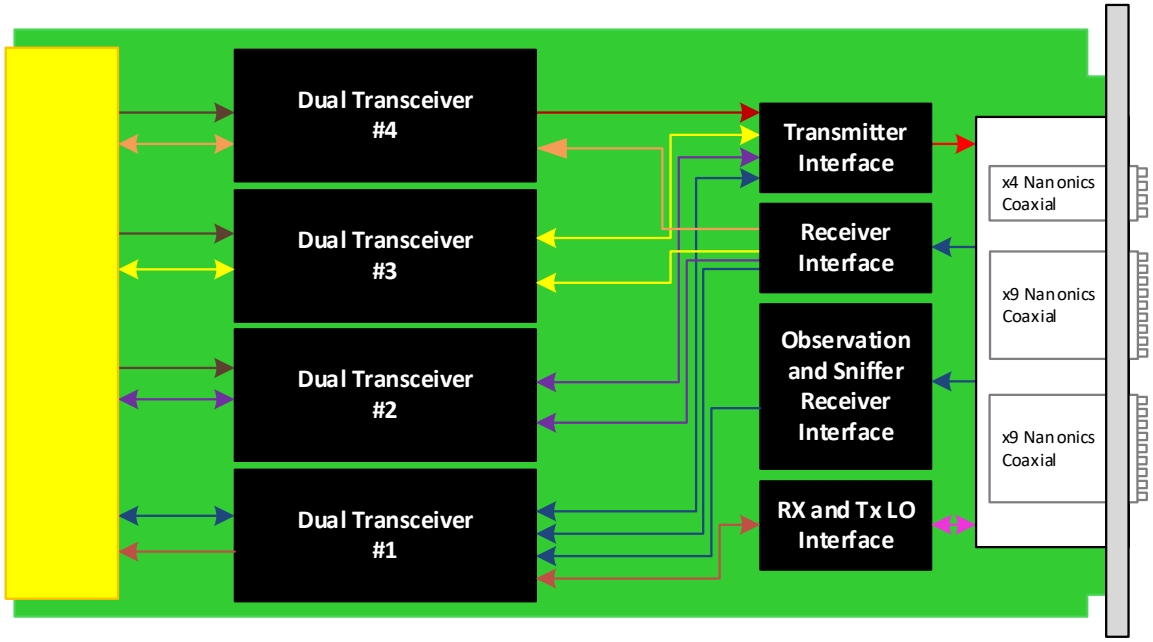


Figure 3: RF Sub-system Block Diagram

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

The AMC597 is compatible with Analog Devices design tools for AD9371.

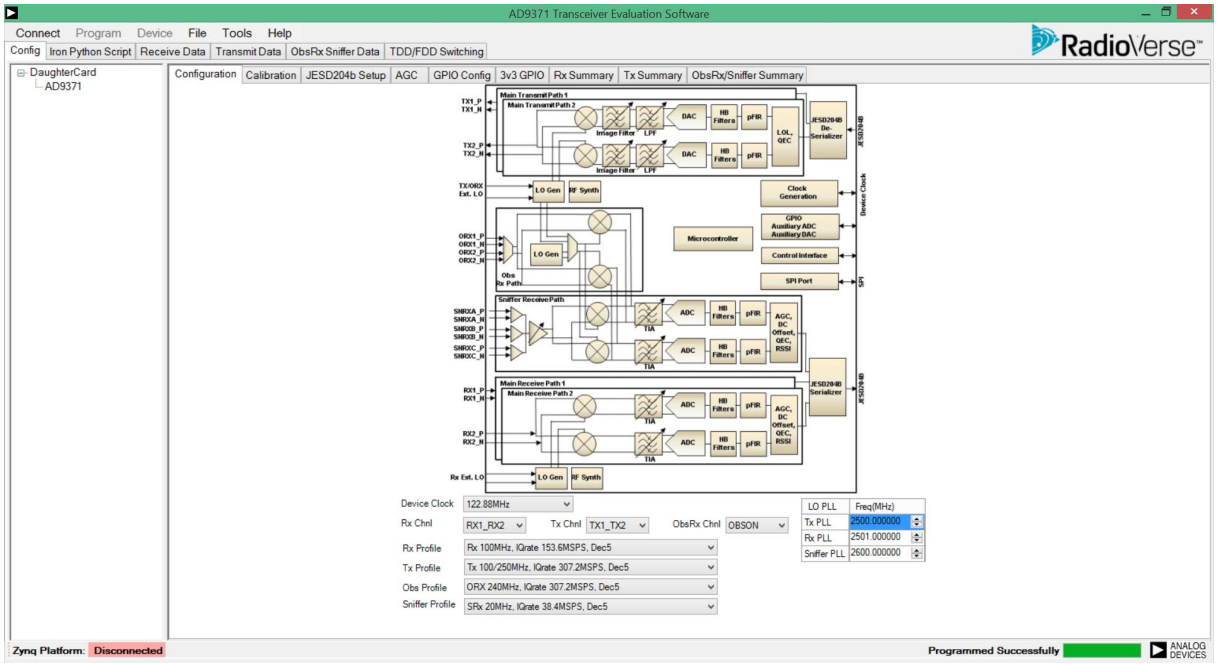


Figure 4: Compatible Analog Devices

Specifications

Architecture		
Physical	**Dimensions**	Single Module, full-size
		Width: 2.89” (73.5 mm)
		Depth: 7.11” (180.6 mm)
Type	**AMC FPGA ADC/DAC**	Xilinx UltraScale™ XCKU115 FPGA
		20 GB of DDR4: Two banks 8 GB of DDR4 64-bit wide and one bank 4 GB of DDR4 32-bit wide
		Octal wideband transceivers, AD9371
Standards		
AMC	**Type**	AMC.1 PCIe, AMC.2 Ethernet and AMC.4 SRIO (FPGA programmable)
Module Management	**IPMI**	IPMI v2.0
PCIe	**Lanes**	Single or Dual x4 via FPGA to AMC per ordering option F
SRIO/XAUI	**Lanes**	Single or Dual x4 via FPGA to AMC per ordering option F
SerDes	**Lanes**	x8 via FPGA to AMC Ports 12-15 and 17-20
Ethernet	**GbE**	Dual GbE
Configuration		
Power	**AMC597**	~55W application dependent (may go up to 65W)
Environmental	**Temperature**	See Ordering Options and Environmental Spec Sheet
		Storage Temperature: –40° to +85°C
	Vibration	Operating 9.8 m/s2 (1G), 5-500 Hz
	Shock	Operating 30Gs each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	**Interface Connectors**	x22 Nanonics Coaxial: 1x4 and 2x9 connectors
		MGT RS-232 and FPGA RS-232
		1x mini DisplayPort
	LEDs	IPMI management control
		8 user defined LEDs
	Mechanical	Hot-swap ejector handle
Software Support	**Operating System**	Agnostic
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

AMC597 – ABC-0EF-G0J

A = RF Direct Clock Sampling		G = Clock Holdover Stability
0 = Front panel 1 = Onboard Wideband PLL		0 = Standard (XO) 1 = Stratum-3 (TCXO)
B = MIMO Device	**E = FPGA Speed**	
0 = AD9371 1 = AD9375	1 = Reserved 2 = High 3 = Highest	
C = Front Panel Size	**F = PCIe Option***	**J = Temperature Range and Coating**
1 = Reserved 2 = Reserved 3 = Full-size 4 = Reserved 5 = Reserved 6 = Full-size, MTCA.1 (captive screw)	0 = No PCIe 1 = PCIe on Ports 4-7 2 = PCIe on Ports 8-11 3 = PCIe on Ports 4-11	0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane** 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic**

Notes: *When the Ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SerDes protocols.

**Edge of module for conduction cooled.

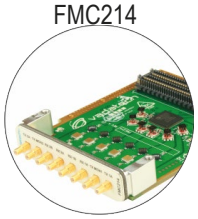
For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Related Products

VT951

- MicroTCA rugged 1U 19” rackmount chassis platform
- Designed to meet MIL-STD-810F, MIL-STD-901D for shock/vibration
- Designed to meet MIL-STD-461E for EMI

FMC214



- Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver
- Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz
- MIMO transceiver is Time Domain Duplex (TDD) and Frequency Domain Duplex (FDD) compatible

AMC599

- Xilinx UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS or quad ADC at 3.2 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

Contact

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